Lab 2: Universal Logic Gates

**Tasks to do:**

**1. Complete all the tables & figures (F1. to F3.)**

**2.** Attach the relevant screenshots of simulated circuits.

## Experimental Data

|  |  |
| --- | --- |
| XOR by NAND | XNOR by NAND |

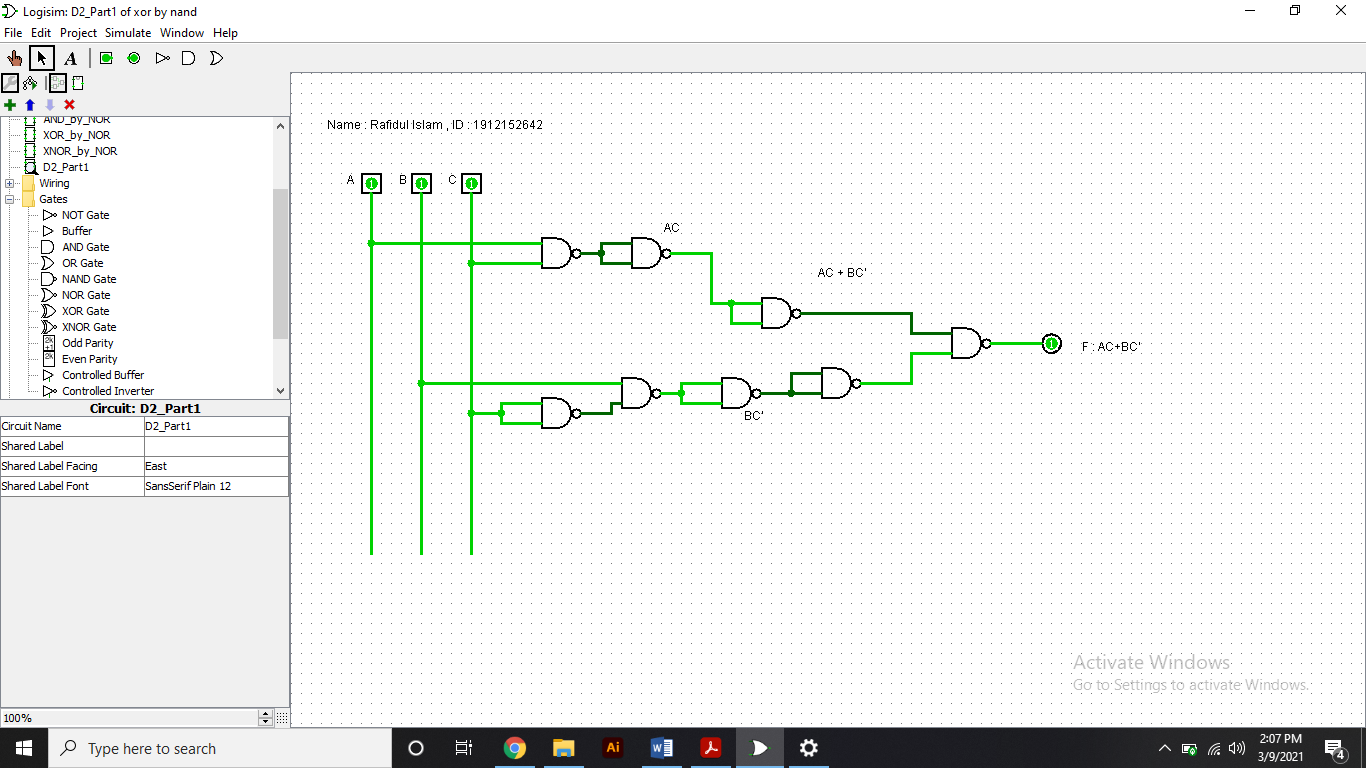
**Figure F1: Implementation of XOR and XNOR using NAND gates**

|  |  |  |  |
| --- | --- | --- | --- |
| NOT by NOR | OR by NOR | | AND by NOR |
| XOR by NOR | | XNOR by NOR | |

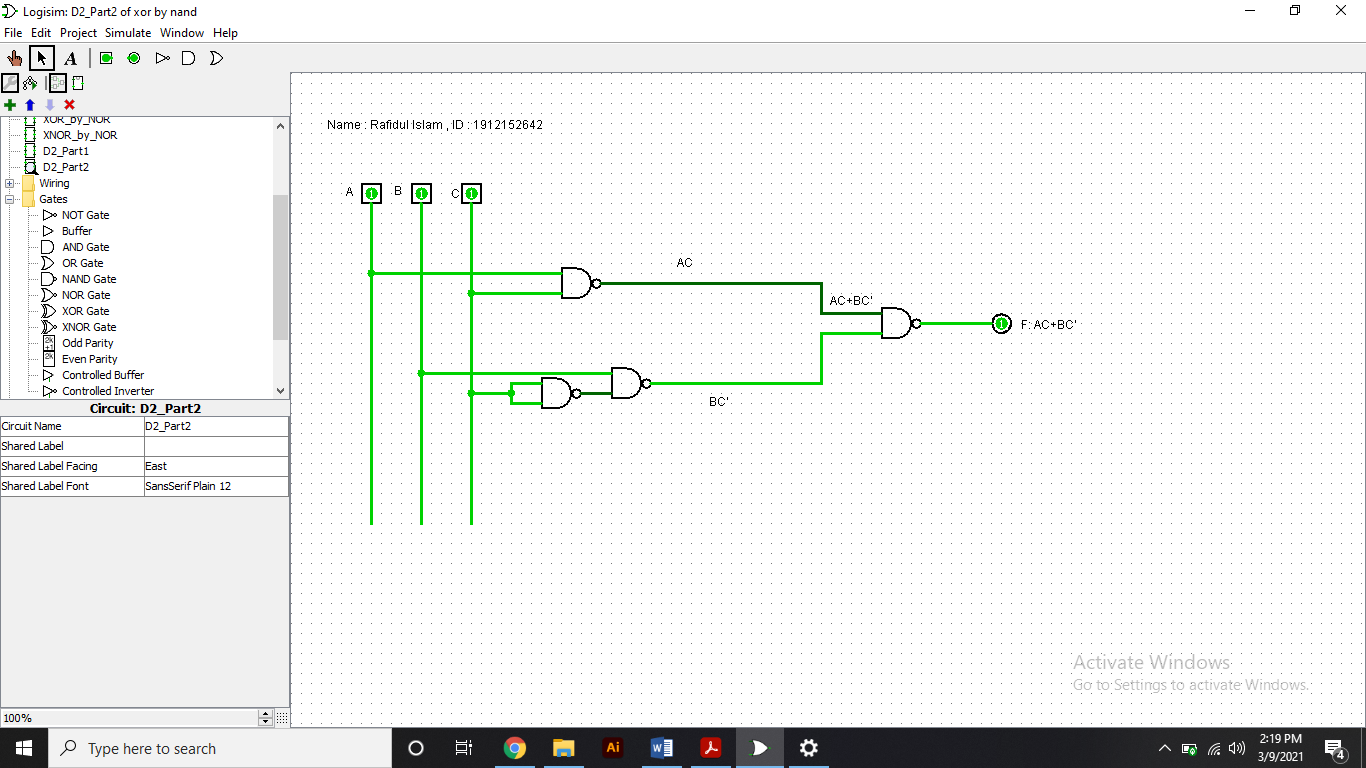
**Figure F2: Implementation of NOT, AND, OR, XOR and XNOR using NOR gates**

|  |  |  |  |
| --- | --- | --- | --- |
| **A B C** | **I1** = AC | **I2** = BC’ | **F** = I1 + I2 |
| 0 0 0 | 0 | 0 | 0 |
| 0 0 1 | 0 | 0 | 0 |
| 0 1 0 | 0 | 1 | 1 |
| 0 1 1 | 0 | 0 | 0 |
| 1 0 0 | 0 | 0 | 0 |
| 1 0 1 | 1 | 0 | 1 |
| 1 1 0 | 0 | 1 | 1 |
| 1 1 1 | 1 | 0 | 1 |

**Table F1: Truth table of combinational circuit in Figure B2**

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**Part 1 of D2 by NAND**

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**Part 2 of D2 by NAND**